1200 E California Blvd,
Pasadena, CA 91126

Benjamin Boone

bboone@caltech.edu
(757) 979-7484

LinkedIn

EDUCATION

California Institute of Technology (Caltech) — **Pasadena, CA**

- Bachelor of Science in Electrical Engineering — Expected June 2028
- Relevant Coursework (**completed** & in progress): — **GPA: 4.0**

  Microwave Circuits and Antennas, Mixed-mode Integrated Circuits, High Frequency Systems Lab, Analog Circuit Design, Analog Lab, **Digital Logic and Embedded Systems**, **Signal Processing**, **Physics of Electrical Engineering**, **Electronic Systems Prototyping**, **Electronics Laboratory**, **Space Electronics,** Mathematics of Electrical Engineering

SKILLS

Programming: C, Python, AVR Assembly, MATLAB
Hardware & Embedded Systems: Altium Designer, PCB Layout, schematic capture, embedded systems, component selection, soldering
RF & Circuit Design: Cadence AWR Microwave Office, LTSpice, RF/microwave circuit design, S-parameter analysis, impedance matching
Test & Measurement: Vector Network Analyzer (VNA), oscilloscope, spectrum analyzer, multimeter
Electromagnetic Simulation: COMSOL Multiphysics, ANSYS Lumerical (MODE, FDTD), Palace, Gmsh
Semiconductor Fabrication: Electron Beam Lithography, PECVD, e-beam evaporation, plasma etching, SEM, ellipsometry, profilometry

PROJECTS

ISS Biological Payload Imaging System — **Pasadena, CA**
Caltech, National Geographic, Brinson Exploration Hub — March 2026 – June 2026

- Designed and integrated the optical imaging subsystem for a biological payload scheduled to fly aboard the International Space Station, performing optics analysis, lens selection, LED illumination design, image processing, subsystem integration, and qualification (TRL 4-5).

Microwave Circuit Design, Simulation, and Characterization — **Pasadena, CA**
EE 153 - Microwave Circuits and Antennas, Caltech — January 2026 – March 2026

- Designed and optimized microwave components including couplers, filters, matching networks, oscillators, and LNAs in Cadence AWR Microwave Office, performing S-parameter, gain, and noise analysis; experimentally characterized circuits using VNA and spectrum measurements to validate S-parameter and gain performance.

2D Chip-scale Blue Light Optical Phased Array — **Provo, UT**
IMMERSE-X Research Program, BYU Electrical & Computer Engineering — June 2026 – Present

- Designing a 2D silicon nitride integrated optical phased array for visible (488 nm) operation using ANSYS Lumerical MODE and FDTD, including waveguide routing, beam steering architecture, grating emitters, and photonic device optimization.

High Altitude Balloon for Atmosphere Characterization — **Pasadena, CA**
EE 154 a - Practical Electronics for Space Applications, Caltech — January 2026 – March 2026

- Designed and built a multi-sensor, time-synchronized data acquisition system for a high-altitude balloon mission, implementing fault-tolerant embedded electronics and qualifying the subsystem for near-space operation via thermal vacuum testing and space-environment design methodologies (TRL 3–4).

Volumetric POV Display — **Pasadena, CA**
Personal Project – Tim Ryan Makerspace, Caltech — April 2026 – Present

- Developing a volumetric persistence-of-vision (POV) display using an ESP32, embedded C, and COTS electronics, including schematic capture, and integrating LED driver circuitry, motor synchronization, sensors, and real-time firmware to generate 3D images.

8-bit CPU and Pinball Machine — **Pasadena, CA**
EE 10 ab - Digital Logic and Embedded Systems, Caltech — January 2025 – June 2025

- Architected and implemented a custom 8-bit CPU in ABEL, including the instruction set, control unit, ALU, and memory interface.
- Developed low-level AVR Assembly firmware to control an electromechanical pinball system, interfacing with sensors and actuators and performing hardware-level debugging with laboratory instrumentation.

EXPERIENCE

Caltech, Quantum Photonics Group — **Pasadena, CA**
SURF Undergraduate Research Fellow, Mentor: Oskar Painter — February 2025 – Present

- Designed superconducting microwave circuits using COMSOL to optimize electromagnetic fields and device performance. Used Python-based simulation tools and FEA to evaluate circuit behavior and fabrication tradeoffs.

Kavli Nanoscience Institute, Caltech — **Pasadena, CA**
Lab Assistant — October 2025 – Present

- Performed semiconductor nanofabrication and process characterization using electron beam lithography, thin-film deposition, SEM, profilometry, and PECVD while developing SPC procedures for select tools to improve manufacturing repeatability.

LEADERSHIP

The Church of Jesus Christ of Latter-day Saints, *Full-time Missionary, Various other roles* — August 2022 – 2024, Present
Boy Scouts of America, *Eagle Scout* — June 2020
The Caltech Y, *Executive Committee Member* — October 2024 - Present